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Research Article

Multi-channel Vibration Signal Acquisition System Based on ARM

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Keywords

Vibration,
Signal,
Acquisition,
Advanced RISC machine,
Analog-to-digital converter.

Abstract

In modern industrial scenes, it is very important to ensure the safe operation of machinery equipment. Therefore, it is necessary to detect the state of the mechanical equipment. There are many kinds of signals for mechanical equipment state detection and fault diagnosis. The most common of signals is mechanical vibration signals. This article uses the STM32F767 and the built-in ADC of the controller to achieve multi-channel acquisition of vibration signals. After experimental test verification, the acquisition accuracy meets the requirements. The peak-to-peak voltage deviation is less than 2%. The synchronization between adjacent channels also meets the requirements, and the acquisition error is less than 1%.

1. Introduction

Vibration signal is an important technical parameter for detecting mechanical equipment. Many faults are reflected in abnormal vibration signals [1]. At present, the systems that use embedded technology to collect vibration signals have some problems [2]. The advanced system has complex structure, difficult operation, and high price. The low-side data acquisition device does not meet the requirements in accuracy and their versatility is poor [3]. In view of the above problems, this article chooses to use the built-in analog-to-digital converter (ADC) of the STM32F767IGT. Through reasonable configuration of ADC performance parameters to realize multi-channel, high-precision data acquisition. This is not only conducive to reducing costs, but also has a certain practicability [4].

2. Hardware Design of System

2.1. STM32 Overall Overview

This article chooses the high-performance advanced RISC machine (ARM) Cortex-M7 32-bit RISC core STM32F767 as the main controller, and its operating frequency is up to 216MHz. The Cortex-M7 core has a floating-point unit (FPU) that supports Arm double-precision and single-precision data processing instructions and data types. It also implements a complete set of digital signal processing (DSP) instructions and a memory protection unit (MPU) to enhance the security of the application [5].

STM32F767 has three 12-bit ADCs, two digital-to-analog conversions (DAC), one low-power real time clock (RTC), twelve general-purpose 16-bit timers, including two pulse width modulation (PWM) timers for motor control [6], two general-purpose 32-bit timers, and a true random number generator. These resources can help us configure the built-in 12-bit ADC well to meet the vibration signal acquisition accuracy and ensure low cost [7].

For most vibration signals, the maximum sampling frequency of 10kHz can meet actual needs. Higher sampling frequencies are generally used in ADCs with more than 12 bits. For its built-in 12-bit ADC, the maximum conversion rate is 2.4MHz, that is, the minimum conversion time is 0.41μs when the ADC clock frequency is set to the maximum

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36MHz, and the sampling period is set to the minimum of 3 clock cycles of ADC to get. This fully meets the general requirements for data collection frequency. At the same time, each ADC contains 19 multiplexed channels, which can measure signals from 16 external sources, two internal sources and V_{BAT} channels. The number of channels also fully meets the sampling requirements. The ADC of each channel has multiple working modes to choose from, namely: single conversion, continuous conversion, scan conversion and intermittent conversion [8].

2.2. A/D data Acquisition

The role of ADC is to convert analog signals into digital signals. Most ADCs input voltage signals from external sensors and output converted digital signals [9]. The data acquisition methods discussed in this article are all based on the internal analog-to-digital converter of STM32F767.

The key technical parameters of the ADC are as follows: sampling time, sampling accuracy, resolution, and conversion rate.

2.2.1. Sampling Time

As shown in Figure 1, the ADC needs a stable period of time T_{STAB} before starting the accurate conversion. And then ADC waits for the trigger signal. When the conversion is turned on, after the total conversion time, the EOC bit is set to 1. The conversion result is saved to the ADC data register. Finally, use software to clear the EOC bit and wait for the next conversion.

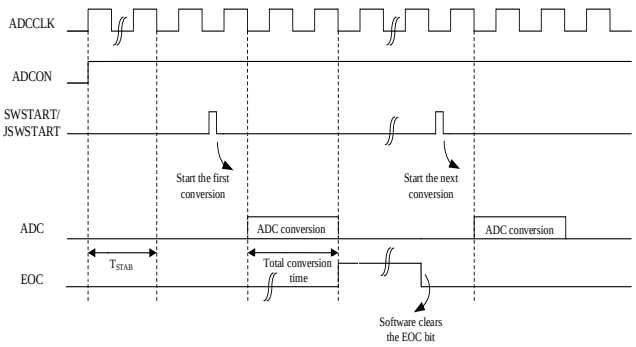

Figure 1. ADC sequence Diagram

For the channel to be converted inside the ADC, the first thing to determine is the sampling time. The ADC will sample the input voltage in multiple ADCCLK cycles. The number of cycles of the sampling time can be modified by modifying the configuration bits of the register. It can be configured as 3, 15, 28, 56, 84, 112, 144 or 480 cycles. Each channel can use different sampling time for sampling [10].

The conversion time of a single channel of the ADC can be calculated as Eq. (1)

$$T_{con} = Sampling\_time + 12\text{cycles} \quad (1)$$

where, T_{con} is the total conversion time, the unit is the number of cycles; 12 cycles correspond to the number of ADC bits.

Therefore, for an ADC configured with multiple channels for acquisition, the total conversion time of the ADC is (Eq. (2))

$$T = \frac{N \times T_{con}}{ADCCLK} \quad (2)$$

where, N is the number of channels; and $ADCCLK$ is the ADC clock frequency, this clock comes from the APB2 clock divided by the programmable prescaler, Hz.

The $ADCCLK$ maximum configuration frequency is 36MHz. Exceeding this frequency will cause the sampling data accuracy to drop significantly.

For each channel to be converted, it is necessary to make the sampling time as long as possible to ensure that the data has a higher accuracy. But at the same time this will also reduce the conversion rate of the ADC. Especially when using multiple channels for data acquisition, a reasonable configuration of the sampling time becomes the key. This article chooses to configure the sampling time of the ADC as 3 cycles to maximize the conversion rate of the ADC, reduce the total conversion time of the ADC, and also meet the accuracy required by most data acquisition scenarios.

2.2.2. Sampling Accuracy

The ADC input range of STM32F767 is $V_{REF} \leq V_{IN} \leq V_{REF+}$, and the input range of V_{REF} is 1.8V-V_{DDA}. V_{DDA} is an analog power input, equal to V_{DD}, when running at full speed, $2.4V \leq V_{DDA} \leq V_{DD}$ (3.6V). When running at low speed, $1.8V \leq V_{DDA} \leq V_{DD}$. When the reference voltage value is set to 3.3V, if the acquisition accuracy of the 12-bit ADC is used to acquire 3.3V voltage, its recognition accuracy is 0.8mV under ideal conditions.

STM32F767 has an internal reference voltage V_{refint}. It is equivalent to a standard voltage measurement point, which is connected to channel 17 of ADC1 internally(ADC1_IN17). That is to say, we can calibrate the drift of the values collected by the other ADC channels through this channel. For an ADC with a sampling accuracy of 12 bits, that is Eq. (3):

$$V_{chx} = AD_{chx} \times V_{refint} / AD_{refint} \quad (3)$$

where, V_{chx} is the calculated actual voltage value, V; AD_{chx} is the ADC channel sampling value that needs to be measured; V_{refint}=4095×1.2/3.3=1489mV for a sampling accuracy of 12 bits, where 1.2 is the voltage of the standard voltage measurement point, and it will not change with the change of external power supply voltage; and AD_{refint} is the ADC value collected by the seventeenth channel of ADC1(ADC1_IN17).

In terms of improving stability, it is generally divided into two methods: hardware and software. Using the hardware method, we can connect a 1μF capacitor or select a filter between the ADC pin and GND. The way of software is to choose a software filter that matches with its own system.

2.2.3. Sampling Accuracy

This article chooses to use the PWM timer to trigger the ADC for sampling. So that we can adjust the ADC sampling frequency we need by controlling the trigger frequency of the PWM timer. For STM32F767 timers, in addition to TIM6 and TIM7, other timers can be used to generate PWM output. Among them, the timers TIM1 and TIM8 can generate up to 7 outputs at the same time.

The overflow time of the timer is (Eq. (4)):

$$T_{\text{out}} = \frac{(arr+1)\times(psc+1)}{TIMCLK} \tag{4}$$

where, *arr* is the auto-load value; *psc* is the frequency division coefficient; and *TIMCLK* is the input clock frequency of the timer, Hz.

The trigger frequency of the timer is the reciprocal of the overflow time. We use it to trigger the ADC. So that the sampling frequency of the ADC is the timer trigger frequency. The total conversion time of the ADC should be less than the overflow time of the timer.

3. Software Design of System

3.1. DMA Technology Overview

Direct memory access (DMA) transfer copies data from one address space to another address space [11]. It provides high-speed data transfer between peripherals and memory or between memory and memory. As the core of system operation, central processing unit (CPU) has functions such as data transfer, calculation, and control program transfer. The independent DMA channel provides us with a data path, which can directly copy data A to B without CPU processing. The role of DMA is to prevent excessive consumption of CPU resources when a large amount of data is transferred. So that the CPU can focus more on more practical operations, calculations, and control.

At the beginning of the DMA transfer work, the authority of the bus must be given to the DMA module first, and then the authority of the bus will be returned to the CPU at the end. The complete DMA transfer includes: (1) request; (2) response; (3) transfer; (4) end. Figure 2 shows the DMA data transfer process.

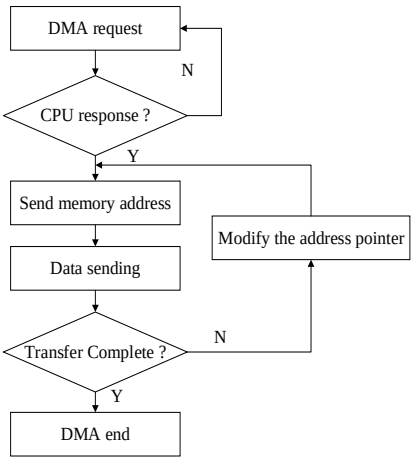

Figure 2. DMA data transfer process diagram

3.2. DMA Module in STM32F767

The STM32F767 contains two DMA controllers with a total of 16 data streams. Each DMA controller is used to manage the memory access requests of one or more peripherals. Each data stream of DMA can have up to 8 channels (or requests) in total. Each data stream channel is also equipped with an arbiter to handle the priority between different channels of DMA. In each transmission, you can also configure the exclusive size. The channel with the exclusive size has the highest priority. After the data specified by the exclusive size is transmitted, the transmission will stop and transfer to the next priority channel.

For data transmission, the first thing that needs to be determined is the core parameters required for DMA transmission. They are the data source address, the destination address of the data transmission location, the amount of data transmitted, and the number of data transmissions.

When the user configures the parameters, mainly configures the source address, destination address, and the amount of data to be transferred, the DMA controller will start the transfer. When the required amount of data transfer is completed, the DMA transfer will be terminated and an interrupt will be issued to the peripheral. When DMA is set to cyclic transmission mode, DMA will restart DMA transmission every time it reaches the end of the transmission.

3.3. Software Module

The main work of this article is data acquisition and data transmission. First of all, we should complete the driver initialization before data acquisition. It includes A/D initialization, DMA initialization and system initialization. The initialization of A/D is a crucial step in the acquisition process. This article has enabled four ADC conversion channels, and the converted data is stored in the register ADC_DR, which must be initialized before each conversion. The DMA initialization is performed because the conversion data saved in the previous register is transferred to the memory. It improves the data transmission efficiency. System initialization includes system clock initialization, interrupt source configuration, GPIO port configuration, timer initialization and parameter configuration. The process is that the system starts and enters the initialization process. When the initialization is completed, the AD starts to enter the data acquisition process. Then the system transfers the data through DMA, and continues to loop until the system issues a stop command. Figure 3 is a flow chart of data collection.

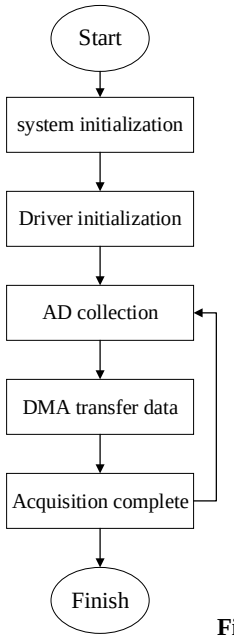

Figure 3. Data collection flow chart

4. System Debugging

4.1. Voltage Peak-to-peak Error Test

In order to verify the multi-channel acquisition stability and measurement accuracy of the ADC built-in STM32F767 after the configuration of this article. This article uses the GFG-8019G signal generator as the signal source to collect and test the sine wave that it sends out in line with the acquisition range. The collected test results are shown in Table 1 below. The signal frequency in Table 1 is 50Hz. The sampling frequency is 800Hz. And the DS1102C oscilloscope is added for synchronous acquisition to compare the results.

Table 1. Sine wave voltage peak-to-peak test

Given value,V	Measured by DS1102C,V	Measured by STM32F767, V	error, %
0.5	0.510	0.513	0.585
1	1.040	1.023	-1.661
1.5	1.510	1.512	0.132
2	2.010	2.021	0.544
2.5	2.520	2.531	0.435
3	2.980	2.957	-0.778

The results show that the built-in ADC of STM32F767 can perform multi-channel data acquisition under the condition of reasonable configuration. And it meets certain accuracy requirements. Voltage peak-to-peak error is within 2%.

4.2. Synchronization Test

When using multiple channels of the ADC for data collection, it needs to be configured in scan mode, that is, multiple channels are collected cyclically in the order of configuration. At the same time, there is a certain signal crosstalk between adjacent channels. These factors make it unavoidable that there is a certain delay between adjacent acquisition channels. This will not only cause a certain error, but also affect the synchronization of the acquisition. These differences will increase the error of later signal processing, so it is a very important issue to examine the synchronization of adjacent acquisition channels.

In order to verify the synchronization of ADC multiple channel acquisition after configuration in this article. This article uses channel 4 and channel 5 of ADC3 in STM32F767 and uses GFG-8019G signal generator as the signal source to send out a sine wave that meets the acquisition range. Then perform the acquisition synchronization test. Table 2 shows the acquisition error of two adjacent channels in a test cycle. The signal frequency in Table 2 is set to 100Hz. The sampling frequency is set to 1600Hz. And the offset voltage is 0.5V.

Table 2. Comparison table of adjacent channel voltage value

Channel 4 voltage.(mV)	Channel 5 voltage.(mV)	error.(%)
668	667	-0.15
563	564	0.18
613	615	0.33
849	845	-0.47
1165	1170	0.43
1538	1549	0.72
1904	1919	0.79
2242	2253	0.49
2478	2468	-0.40
2586	2585	-0.04
2485	2484	-0.04
2241	2234	-0.31
1942	1932	-0.51
1575	1574	-0.06
1214	1206	-0.66
904	897	-0.77

4.3. Screen Display

EmWin was developed to provide an efficient processing method for any application with graphical LCD operation to aid in graphical interface design of the user interface. The design and development of the interface is based on a number of directly available functions (apis) provided by emWin.

In this paper, emWin is used for the subsequent page development and design, and the multi-channel data collection is processed visually. The main function of the page is to display waveform. By using appropriate proportions and initializing the horizontal and vertical axes, the waveform can be well studied. Figure 4 shows the screenshots of waveform display of channel 4 and channel 5. In the figure, the GFG-8019G signal generator is used as the signal source. The set voltage peak-to-peak value is 2V, bias voltage is 0.5V. As can be seen from the figure, the waveforms of the two channels basically coincide completely, making the synchronization of the channels more intuitive.

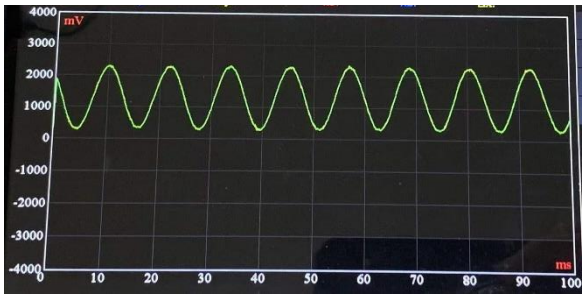

Figure 4. Screen display screenshot

5. Conclusions

According to the requirements of high precision and high speed in the data acquisition system, this article chooses to use STM32F767 as the main control chip. And the system uses the built-in ADC for data acquisition. It has verified its multichannel synchronous analog-to-digital conversion capability, and has a certain degree of flexibility. At the same time, the number of channels, sampling time, and sampling frequency can be changed. After experimental testing, the voltage peak-to-peak error is less than 2%. The frequency test accuracy and synchronization of multi-channel acquisition also meet the requirements of most of the acquisition process.

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